What is claimed is:

1. An HVR reticle which is configured for registration with an LVR reticle, said HVR reticle comprising:

an array of die; and

a plurality of scribes which are wrapped around each of said dies of said array of die.

2. An HVR reticle as defined in claim 1, wherein said array of die is in a two by two formation.

3. An HVR reticle as defined in claim 1, wherein said plurality of scribes includes a plurality of X scribes and a plurality of Y scribes.

4. An HVR reticle as defined in claim 3, wherein each said X scribe is positioned below each said die of said array of die.

5. An HVR reticle as defined in claim 3, wherein each said Y scribe is positioned to the right of each said die of said array of die.

6. An HVR reticle as defined in claim 1, wherein each said scribe includes an N-type transistor or a P-type transistor.

7. An HVR reticle as defined in claim 1, wherein each said scribe includes an N-type transistor, but does not include a P-type transistor.

8. An HVR reticle as defined in claim 1, wherein each said scribe includes a P-type transistor, but does not include an N-type transistor.

9. A method of forming an HVR reticle which is configured for registration with an LVR reticle, said method comprising the steps of:

a) laying an array of die; and

b) wrapping a scribe around each die of said array of die.

10. A method as defined in claim 9, wherein step (b) further comprises the steps of:

b1) wrapping an X scribe around each die of said array of die; and

b2) wrapping a Y scribe around each die of said array of die.

11. A method as defined in claim 9, further comprising the step of:

c) splitting each said scribe such that each said scribe includes either an N-type transistor or a P-type transistor as necessary.

12. A method of preparing a wafer comprising the steps of:

a) providing an LVR reticle which includes different dies laid out in an array, each said die of said LVR reticle having at least one scribe wrapped therearound;

b) providing an HVR reticle which includes identical dies laid out in an array, each said die of said HVR reticle having at least one scribe wrapped therearound;

c) exposing said HVR reticle on the wafer;

d) blading out one of said dies of said LVR reticle;

e) aligning said at least one scribe of said bladed out die of said LVR reticle with said at least one scribe of one of said dies of said HVR reticle; and

f) exposing said bladed out die of said LVR reticle with said one die of said HVR reticle.

13. The method as defined in claim 12, further comprising the steps of:

a) splitting said scribes of said LVR reticle such that each said scribe of said LVR reticle either has a first back-end metal or a second back-end metal such that an area covered by said scribes of said LVR reticle is reduced; and

b) splitting said scribes of said HVR reticle such that each said scribe of said HVR reticle either has an N-type transistor or a P-type transistor such that an area covered by said scribes of said HVR reticle is reduced.